## REMARKS

Claims 1-28 are pending and claims 13 and 14 stand rejected. Applicant appreciates the recognition of the allowable subject matter in claims 1-12 and 15-28. However, the Office action objected to the drawings under 37 CFR § 1.83(a) for failing to show every feature of the claimed invention specified in the claims. The Office action also rejected claims 13 and 14 under 35 USC § 102(b) as being anticipated by Naffziger U.S. Pat. 6,075,386 (hereinafter "Naffziger").

In response, Applicant respectfully traverses the drawing objections, requests that independent claim 13 be amended and claim 14 be cancelled in accordance with the amendments, and traverses the rejections in light of amended claim 13.

Drawing objections

In regards to the objection to the drawings as failing to show every feature of the claimed invention specified in the claims 15 and 16 under 37 CFR § 1.83(a), the Office action states that:

> ... *the first transistor having a channel coupled between the logic transistor and a low voltage source, and a gate coupled with a comparator; and the second transistor having a channel coupled between the output and a low voltage source and a gate coupled with the comparator*, in claims 15 and 16 respectively, must be shown or the feature(s) cancelled from the claims(s).

Applicant respectfully suggests that these features of claims 15 and 16 are shown in the drawings and that a person of ordinary skill in the art would recognize an embodiment of these features upon review of figures 1B and 2. In particular, the "first transistor" (element 262) has a channel coupled between the "logic transistor" (element 248) and a "low voltage source", which is symbolized by a common symbol for a low voltage source or ground comprising a downward pointed arrow as described in the "LEGEND" of figure 2. The "comparator" (element 137 shown in figure 1B) is coupled with the gate of the "first transistor" (element 262) when "delay" (element 138) activates "NOR gate" (element 133).

Similarly, the "second transistor" (element 264) has a channel coupled between the "output" of the normal input gate (element 130), which is the node shown between transistors 268 and 245, and a "low voltage source", which is symbolized by the downward pointed arrow

as described in the "LEGEND" of figure 2. The "comparator" (element 137 shown in figure 1B) is coupled with the gate of the "second transistor" (element 264) when "delay" (element 138) activates "NOR gate" (element 133). Thus, Applicant respectfully requests that this objection to the drawings be withdrawn.

Claim rejections under 35 USC § 102

Claims 13 and 14 stand rejected under 35 USC § 102(b) as being anticipated by Naffziger. Applicant respectfully suggests that the rejections with respect to amended claim 13 is traversed in accordance with the amendments and the following remarks.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single reference.[1] Furthermore, the identical invention must be shown in as complete detail as is contained in the claim.[2]

In regards to the amended independent claim 13, the Office action fails to establish a prima facie case of anticipation by Naffziger because citations of Naffziger provided as support for the rejections fail to describe, suggest or teach "each and every element as set forth in the claim[s]".

Applicant, in the above claim amendments, has respectfully requested that the limitation(s) of claim 14 be added to claim 13 with the phrase "a normal input path, evaluation clock" being replaced by "a system clock" and that claim 14 be cancelled. As a result, amended claim 13 states:

> ... a pre-charge circuit to pre-charge a dynamic node before the data signal is evaluated; a logic transistor having a gate coupled with the data signal to discharge the dynamic node when the normal input gate is activated; and an output to couple a voltage source to the latch based upon a charge on the dynamic node; ***wherein the data signal and a system clock are gated directly to the normal input gate to evaluate the data signal.***-(emphasis added).

Thus, Applicant respectfully requests that the response to with regards to amended claim 13 be considered responsive to the rejections of both claims 13 and 14 in the Office action. With regards to the rejection of amended claim 13, the Office action states:

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[1] *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 U.S.P.Q.2d 1051, 1053 (Fed. Cir. 1987).
[2] *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236, 9 U.S.P.Q.2d 1913, 1920 (Fed. Cir. 1989).

> ... In claim 13, Naffziger teaches all claimed features in Fig. 4, a normal input gate for gating a data signal (input to logic 108, see Fig. 1) to a latch of the scanable latch circuit, the normal input gate comprising: a pre-charge circuit (402) to pre-charge a dynamic node (410) before the data signal is evaluated; a logic transistor (inherent, a logic gate inside 108 not shown) having a gate coupled with the data signal (input to 108) to discharge the dynamic node when the normal input gate is activated (input mode); and an output (OH) to couple a voltage source ($V_{DD}$) to the latch based upon a charge on the dynamic node (when 402 is closed or conducting).
>
> In claim 14, Naffziger further teaches ***the normal input gate of claim 13, wherein the data signal (input to 108) and a normal input path (OH), evaluation clock (100) are gated directly to the normal input gate (Fig. 4) to evaluate the data signal***....-(emphasis added).

However, Naffziger does not describe "a system clock" as being "gated directly to the normal input gate to evaluate the data signal". In fact, in figure 4, Naffziger describes the clock signal as a separate clock signal (RCK 400) derived from the main clock (element 100) and illustrates the separate clock signal (RCK 400) as being coupled with the "normal input gate" of figure 4 via a transistor (element 402) controlled via a delay circuit (element 408). Naffziger (col. 4, lines 5-12 and lines 31-33) states:

> ... For the gate in FIG. 4, ***two separate clock signals are derived from the main clock 100. A reset clock RCK 400 controls a precharge transistor 402.*** An evaluate clock ECK 404 controls an evaluate transistor 406. ***When clock 100 goes high, RCK 400 pulses low for a time determined by a delay circuit 408 and then returns high.*** RCK 400 pulses low just long enough to ensure that precharge transistor 402 completely charges the evaluation node NOH 410.... At the same time that precharge transistor 402 turns off, ECK 404 goes high and evaluate transistor 406 is turned on. ***After clock 100 goes low (delay 408), NCKD 409 goes high and the evaluation transistor 406 turns off.... After delay 408, NCKD 409 goes low, turning transistor 414 off and transistor 418 on, which pulls RCK high, which turns off the precharge transistor 402.*** When clock 100 goes from high to low, transistor 412 is turned off and transistor 416 is turned on, so that RCK remains high. ***Delay 408 may be a series of inverters (even number) or may be a simple RC filter.***-(emphasis added).

On the other hand, the present application, in several embodiments, specifically describes the connection between the "system clock" and the "normal input gate" as "coupled directly" and illustrates the same in figures 1B and 2. The "DETAILED DESCRIPTION OF EMBODIMENTS" section of this application (pars. 25, lines 20-24) states:

> ... ***Advantageously***, because scan path 142 and normal input path 140 are separate paths, ***system clock 103 and data 113 may be coupled directly to the input of normal input gate 130, potentially gating data 113 to combinational logic circuit 160 without introducing any gate delays beyond the gate delay associated with normal input gate 130.***-(emphasis added).

Further, the "DETAILED DESCRIPTION OF EMBODIMENTS" section of this application (par. 43, lines 17-20) states:

> ... ***Normal input gate 130 may advantageously receive system clock 103 and data 113 as direct inputs. For instance, in many embodiments, few or no gates reside between the input pin of system clock 103 and normal input gate 130, reducing delays associated with normal input path 140.***-(emphasis added).

In sum, Naffziger not only teaches a separate clock with the disadvantages of delays in generating a separate clock signal for the "normal input gate" but also an indirect coupling between the "system clock" and the "normal input gate" via a transistor controlled by a delay circuit. As such, Naffziger does not describe, expressly or inherently, a system clock "gated directly to the normal input gate to evaluate the data signal" as described in amended claim 13. Thus, Applicant respectfully requests that the rejection of amended claim 13 be withdrawn and that amended claim 13 be allowed.

Further, Applicant respectfully suggests that the amendment of claim 13 traverses the objections to the allowable subject matter of claims 15-17 because claims 15-17, being dependent upon amended claim 13, incorporate the limitations of amended claim 13. Thus, Applicant respectfully requests that these objections be withdrawn and claims 15-17 be allowed.

## CONCLUSION

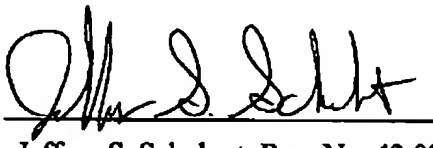
Applicant respectfully traverses the drawing objections by pointing out the features in figures 1B and 2. Applicant also requests entry of the amendments to claim 13 and cancellation of claim 14. With the introduction of the amendments, Applicant respectfully traverses the claim rejections under 35 USC §§ 102. Accordingly, Applicant believes that this response constitutes a complete response to each of the issues raised in the Office action. In light of the amendments made herein and the accompanying remarks, Applicant believes that the pending claims are in condition for allowance. Thus, Applicant requests that the objections and rejections be

withdrawn, pending claims be allowed, and application advance toward issuance. If the Examiner has any questions, comments, or suggestions, the undersigned attorney would welcome and encourage a telephone conference at (512) 288-6635.

No fee is believed due with this paper. However, if any fee is determined to be required, the Office is authorized to charge Deposit Account 50-3295 for any such required fee.

Respectfully submitted,

April 7, 2005
Date



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